BACHELOR OF TECHNOLOGY (CBCS - 2023)
B. Tech. Sem-II Computer Science & Engineering-AI & ML : WINTER : 2024
SUBJECT: DIGITAL ELECTRONICS

Day : Monday
Date : 25/11/2024

W-27702-2024

Time : 10:00 AM-01:00 PM
Max. Marks : 60

N.B.

1) All questions are **COMPULSORY.**
2) Figures to the **RIGHT** indicate **FULL** marks.
3) Assume suitable data **WHEREVER** necessary.
4) Draw neat labeled diagrams **WHEREVER** necessary.

Q.1 Perform the following operation.

a) Add 11011 and 10101 **(02)**
b) Subtract 1010 from 11010 **(02)**
c) Multiply $(2A8)_{16}$ by $(B6)_{16}$ **(03)**
d) Divide $(2C0BE)_{16}$ by $(2A)_{16}$ **(03)**

OR

Q.1 Realize the following function using universal logic. **(10)**
a) X-OR
b) X-NOR

Q.2 Simplify the following expression using Quine Mc Clusky method and realize it using basic gates. **(10)**
$F(A,B,C,D) = \sum m\ (0,1,2,7,8,9,10,11,14,15)$

OR

Q.2 Simplify the following expression using K-map and realize it in universal logic.

a) $F(A,B,C,D) = \sum m\ (1,5,6,12,13,14) + d(2,4)$ **(05)**
b) $F(A,B,C,D) = \pi M\ (0,1,2,3,4,7)$ **(05)**

Q.3 Draw a logic diagram, block diagram, and write a k-map simplification from truth table for full Adder. **(10)**

OR

Q.3 Design a Decimal to BCD priority encoder with the help of truth table. **(10)**

Q.4 Describe the working of D-flip flop and JK-flip flop with the help of truth table. **(10)**

OR

Q.4 Design a Synchronous Mod-6 counter using J-K flip flops. **(10)**

Q.5 Explain Multiplexer controller method for 2-bit Up-Counter. **(10)**

OR

Q.5 Draw a state diagram and ASM chart to detect the sequence 1010. **(10)**

Q.6 Design and Implement Full Adder using Programmable logic Array (PLA). **(10)**

OR

Q.6 Describe SRAM and DRAM with its advantages and disadvantages. **(10)**

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