BACHELOR OF TECHNOLOGY (CBCS - 2023)

B. Tech. Sem-III Computer Science & Business Systems : WINTER: 2025

SUBJECT: COMPUTER ORGANIZATION & ARCHITECTURE

Day : Thursday | Time : 10:00 AM-01:00 PM

Date : 11/12/2025 | **W-29214-2025** | Max. Marks : 60

NB :

1. Assume suitable data, if necessary.
2. Draw neat labelled diagrams WHEREVER necessary.
3. Figures to the right indicate FULL marks for the question.
4. All questions are COMPULSORY.

Q. 1	Draw and explain architecture of 8086.	(10)
	OR	
Q. 1	Explain how Index addressing mode, Immediate addressing mode and Relative addressing mode work?	(10)
Q. 2	Explain IEEE 754 floating point format. Represent $(85.125)_{10}$ number in single and double precision.	(10)
	OR	
Q. 2	Design a flowchart for the restoring division algorithm. Implement this algorithm to perform the division of 11 by 3, demonstrating the steps involved and the result.	(10)
Q. 3	Write a control sequence for the following instructions for single bus organization. ADD (R3), R1. Assuming R1 as destination.	(10)
	OR	
Q. 3	Explain horizontal and vertical microinstruction format.	(10)
Q. 4	Explain briefly about Associate-mapped and set-associate mapped cache.	(10)
	OR	
Q. 4	Compare and contrast the write-through and write-back cache updating policies. Analyze their advantages and disadvantages in terms of performance.	(10)
Q. 5	Illustrate various I/O modes of transfer.	(10)
	OR	
Q. 5	Write a short note on Peripheral devices. With a neat sketch explain the working principle of DMA.	(10)
Q. 6	Demonstrate shared memory parallel processor.	(10)
	OR	
Q. 6	What is cache coherency? Explain MESI protocol.	(10)

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