BACHELOR OF TECHNOLOGY (CBCS - 2023)
B. Tech. Sem-I COMPUTER SCIENCE & ENGINEERING : SUMMER : 2024
SUBJECT: DIGITAL ELECTRONICS

Day : Tuesday
Date : 14/05/2024

S-27609-2024

Time : 10:00 AM-01:00 PM
Max. Marks : 60

N.B.

1) All questions are **COMPULSORY.**
2) Figures to the **RIGHT** indicate **FULL** marks.
3) Assume suitable data **WHEREVER** necessary.
4) Draw neat labeled diagrams **WHEREVER** necessary.

Q.1 Perform the following conversions **(10)**

a) $(A3E)_{16} = (\ )_{10}$
b) $(B92)_{16} = (\ )_{8}$
c) $(635)_{8} = (\ )_{10}$
d) $(10110.101)_{2} = (\ )_{16}$
e) $(86.64)_{10} = (\ )_{2}$

OR

Q.1 Design a digital circuit and truth table for the logic equation **(10)**
$Y = AB\overline{C} + \overline{A}BC + AB + A\overline{C}$
using logic gates.

Q.2 Explain De-Morgan's Theorem in detail with suitable diagram. **(10)**

OR

Q.2 Simplify the following function using K-map and implement using logic gates **(10)**
$F(A,B,C,D) = \sum m(1,5,6,7,11,12,13,15)$

Q.3 Design 4 bit gray to binary code converter. **(10)**

OR

Q.3 Explain 3×8 decoder with truth table and circuit diagram. **(10)**

Q.4 Describe different types of flip-flops with truth tables and circuit diagrams. **(10)**

OR

Q.4 What is Ripple counter? Explain in detail. **(10)**

Q.5 Describe notation of ASM chart. Draw ASM chart and state diagram. **(10)**

OR

Q.5 Design a sequence detector which detects the sequence 1 0 0 1. **(10)**

Q.6 Classify semiconductor memories in detail. **(10)**

OR

Q.6 Describe architecture of PLA with neat block digram.Design full adder using PLA(Programmable Logic Array). **(10)**

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