B. Tech. Sem-VI, (2014 Course), E&TC
winter-2018

B. Tech. Sem -VI (E & TC Engg.) (2014 COURSE) (CBCS) :
WINTER - 2018
SUBJECT : VLSI DESIGN

Day : Thursday
Date : 15/11/2018

W-2018-2514

Time : 10.00 AM TO 01.00 PM
Max. Marks : 60

N. B. :

1) All questions are **COMPULSORY**.
2) Figures to the right indicate **FULL** marks.
3) Draw neat and labeled diagram **WHEREVER** necessary.
4) Use of non-programmable calculator is **ALLOWED**.
5) Assume suitable data, if necessary.

Q. 1 **a)** Using suitable example, discuss Y-chart. **(05)**

b) How SiO_2 is formed? Explain using suitable diagram. **(05)**

OR

Q. 1 How nMOS is fabricated? Explain using suitable diagrams. **(10)**

Q. 2 **a)** What are the small geometry effects on MOSFET? **(05)**

b) For CMOS inverter, V_{DD}=5V, $V_{90\%}$=4.5V, $V_{10\%}$=0.5V, $\mu_n C_{ox}$=20μA/V^2, $(W/L)_n$=10, $V_{T,n}$=1V. Using average current method, calculate τ_{fall} if C_{Load}=5pF. **(05)**

OR

Q. 2 **a)** How MOSFET is operated in saturation region? Define drain current in presence of channel length modulation. **(05)**

b) For CMOS inverter, V_{DD}=3V, $\mu_n C_{ox}$=110μA/V^2, $\mu_p C_{ox}$=50μA/V^2, $(W/L)_n$=7, $(W/L)_p$=20, $V_{T,n}$=0.8V and $V_{T,p}$= - 1V. Calculate τ_{PLH} and τ_{PHL} if C_{Load}=10fF. **(05)**

Q. 3 Draw the diagram and write VHDL code for 4 X 16 decoder. **(10)**

OR

Q. 3 Draw the diagram of 4-bit parallel adder using full adder as a component. Write VHDL code for the same. **(10)**

P. T. O.

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Q. 4		Design FSM for traffic light controller. Write VHDL code for the same.	**(10)**
		OR	
Q. 4	**a)**	Write VHDL code for mod-25 up counter.	**(05)**
	b)	Differentiate different types of FPGA architectures.	**(05)**
Q. 5		Why reduction in switched capacitance helps in reducing power consumption? Discuss in detail.	**(10)**
		OR	
Q. 5		How optimization of switching activities achieve low power operation? Explain.	**(10)**
Q. 6		How scan based design is implemented?	**(10)**
		OR	
Q. 6		What is Adhoc Technique? Describe in detail.	**(10)**

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