BACHELOR OF TECHNOLOGY (CBCS - 2023)
B. Tech. Sem IV Information Technology : WINTER: 2025
SUBJECT: COMPUTER ORGANIZATION & ARCHITECTURE

Day : Thursday | Time : 10:00 AM-01:00 PM
Date : 27/11/2025 | **W-29318-2025** | Max. Marks : 60

NB :
1. Assume suitable data, if necessary.
2. Draw neat labelled diagrams WHEREVER necessary.
3. Figures to the right indicate FULL marks for the question.
4. All questions are COMPULSORY.

Q. 1 Write short notes on the following: (10)

1. Cluster Computing 2) Cloud Computing, 3) Quantum Computing

OR

Q. 1 What is performance metrics? How it explains the parameters for improving performance of the processor? Explain. (10)

Q. 2 Write VHDL code for full adder. Draw block diagram and truth table of full adder. Write important comments in the code. (10)

OR

Q. 2 Write VHDL code for 3:8 Decoder. Draw block diagram and truth table of the circuit. Write important comments in the code. (10)

Q. 3 Explain the hardwired control unit design method of control unit design with complete diagram. Also differentiate between hardwired and microprogrammed control unit. (10)

OR

Q. 3 Write and briefly explain a complete microprogram for the following instruction: (10)

DIV DL, [DI]

Q. 4 Explain the cache write operation with neat figure. What is hit rate and miss rate? Explain (10)

OR

Q. 4 Explain the direct cache memory mapping technique with neat diagram. Give it's advantages and disadvantages. (10)

Q. 5 Explain the distributed memory multiprocessor architecture with neat figure. How it is different from shared memory architecture. Explain. (10)

OR

Q. 5 Explain in detail the supercomputer architecture with suitable diagram. (10)

Q. 6 What is pipeline stall? How it affects the performance of a pipeline? Explain with example. (10)

OR

Q. 6 What is out-of-order execution? How it enhances the performance of a CPU? Explain with example. (10)

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