BACHELOR OF TECHNOLOGY (CBCS - 2023)
B. Tech. Sem-III Computer Science & Engineering AI & ML : WINTER : 2024
SUBJECT: COMPUTER ORGANIZATION & MICROPROCESSORS

Day : Monday
Date : 09/12/2024

W-29208-2024

Time : 10:00 AM-01:00 PM
Max. Marks : 60

N.B.:

1) All questions are **COMPULSORY**.
2) Figures to the right indicate **FULL** marks.
3) Draw neat diagrams **WHEREVER** necessary.
4) Assume suitable data, if necessary.

Q. 1 State features of IAS computers and explain how is DATA and INSTRUCTIONS are stores into memory. **(10)**

OR

Q. 1 Why do we use following components in computer architecture. **(10)**
Instruction Registers (IR), Memory Buffer Register (MBR), General Purpose Registers (GPR), Control Unit

Q.2 Booth's algorithm gives procedure for multiplying binary integers in signed 2's complement representation in efficient way. Draw the flowchart for the algorithm and perform multiplication of (-12) × (-9). Both the numbers are in decimal systems. **(10)**

OR

Q. 2 Why do we use and follow IEEE754 format. Given decimal number is = $(5)_{10}$. **(10)**

Q. 3 Justify cache coherency has integral role in cache management. **(10)**

OR

Q. 3 Consider an 8 – way set associative cache memory unit, where cache size: 16KB, block size: 16 words, word length: 32 bits & physical memory space = 16 GB. Find the number of bits for the TAG, BLOCK & LINE fields? **(10)**

Q. 4 What are the handshaking signals? Explain handshake control of data transfer during input and output operations. **(10)**

OR

Q. 4 Compare Programmed I/O and Interrupt driven I/O. **(10)**

Q. 5 What are the features of Micro Programmed Control Unit? **(10)**

OR

Q. 5 What is address sequencing? Explain the conditional branching and mapping of instruction in it. **(10)**

Q. 6 A non – pipelined single cycle processor operating at 100 MH_z is converted into a synchronous pipelined processor with five stages requiring 25 ns, 2 ns, 15ns and 25ns respectively. The delay of the latches is 05 sec. Find the speed up of the pipeline processor for a large number of instructions. **(10)**

OR

Q. 6 Analyze how instruction pipeline hazards (data, control, structural) affect performance and suggest methods to mitigate them. **(10)**

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