

**BACHELOR OF TECHNOLOGY (CBCS - 2023)**  
**B. Tech. Sem-IV Computer Science & Engineering : WINTER: 2025**  
**SUBJECT: COMPUTER ORGANIZATION & ARCHITECTURE**

Day : Thursday  
Date : 27/11/2025

**W-29275-2025**

Time : 10:00 AM-01:00 PM  
Max. Marks : 60

**N.B.**

- 1) All questions are **COMPULSORY**.
- 2) Figures to the **RIGHT** indicate **FULL** marks.
- 3) Assume suitable data **WHEREVER** necessary.
- 4) Draw neat diagrams **WHEREVER** necessary.

**Q. 1** Differentiate between Von Neumann and Harvard architecture. Illustrate your answer with suitable diagrams and examples. (10)

**OR**

**Q. 1** Differentiate between Computer Organization and Architecture. Explain the functional organization of a computer system with a neat block diagram. (10)

**Q. 2** Describe the structure and working of a Carry Look-Ahead Adder (CLA). How does it overcome the delay in Ripple Carry Adder? (10)

**OR**

**Q. 2** Explain the IEEE-754 floating-point representation. Convert the decimal number (-14.375) into IEEE 754 single and double precision format. (10)

**Q. 3** Explain the key characteristics of RISC architecture. How does it achieve better performance compared to traditional CISC? (10)

**OR**

**Q. 3** What is RTL? Write RTL representation for the instruction: ADD R1, M[1000] and explain each step. (10)

**Q. 4** Compare Fully Associative, Direct and Set Associative Cache Mapping techniques. (10)

**OR**

**Q. 4** A computer has the following specifications: (10)  
Main Memory Size = 256 KB  
Cache Size = 4 KB  
Block Size = 16 Bytes  
Mapping Technique = Direct Mapping

**Calculate:**

- a) Number of blocks in cache
- b) Number of blocks in main memory
- c) Number of tag bits
- d) Size of tag directory (in bits)

**Q. 5** Draw and explain the SCSI architecture. (10)

**OR**

**Q. 5** What is Memory mapped I/O? How it is different from I/O mapped I/O. (10)

**Q. 6** Draw and explain a 5-Stage Pipeline. Calculate the Speed-up and Throughput of it. (10)

**OR**

**Q. 6** Describe the different classification of parallel processors using Flynn's Taxonomy. (10)

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