

**B. Tech. Sem -VIII (E & TC Engg.) (2014 COURSE) (CBCS) :**  
**SUMMER - 2019**  
**SUBJECT : ELECTIVE – II : SYSTEM ON CHIP**

Day : Thursday  
Date : 30/05/2019

Time : 02.30 PM TO 05.30 PM  
Max. Marks : 60

**S-2019-2948**

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**N. B. :**

- 1) All questions are **COMPULSORY**.
  - 2) Figures to the right indicate **FULL** marks.
  - 3) Draw neat and labeled diagram **WHEREVER** necessary.
  - 4) Assume suitable data, if necessary.
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**Q. 1** What is wrong with today's approach to SOC design? **(10)**

**OR**

**Q. 1** What are the implications of improved SOC methodology? How SOC design flow is implemented? **(10)**

**Q. 2** How current SOC design flow is implemented? **(10)**

**OR**

**Q. 2** What will be the impact of semiconductor economics? Discuss tool enhancement with reference to SOC design. **(10)**

**Q. 3** What are the new essentials of SOC design methodology? **(10)**

**OR**

**Q. 3** How to overcome six problems in existing SOC design methods? **(10)**

**Q. 4** Explain reliability and scalability in SOC communication architecture. **(10)**

**OR**

**Q. 4** Describe major decisions in processor-centric SOC organization. **(10)**

**Q. 5** Discuss MP debug and MP trace. **(10)**

**OR**

**Q. 5** What are the issues in memory systems? Discuss any two. **(10)**

**Q. 6** Why is software programmability so central? **(10)**

**OR**

**Q. 6** Explain in brief: Processor scaling model. **(10)**

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