BACHELOR OF TECHNOLOGY (CBCS) (2021-COURSE)

B. Tech. Sem - II Computer Science & Engineering AI & ML : WINTER : 2023

SUBJECT : DIGITAL ELECTRONICS

Day : Thursday | Time : 10:00 AM-01:00 PM

Date : 23-11-2023 | **W-23932-2023** | Max. Marks : 60

N.B.:

1) All questions are **COMPULSORY**.
2) Figures to the right indicate **FULL** marks.
3) Use of non-programmable **CALCULATOR** is allowed.

Q.1 Perform the following operations: **(10)**
a) Add 10011 and 10101
b) Subtract 1110 from 11010
c) Multiply 1101 by 10110
d) Divide 1100 by 11
e) subtract 1010 from 1111

OR

Q.1 Why are NAND and NOR gates called Universal gates? Derive AND and OR gates using NAND and NOR gates. **(10)**

Q.2 Simplify the following expression using Quine Mc Clusky method and realize it using basic gates. **(10)**

$F(A,B,C,D) = \sum m(0,1,3,7,8,9,11,15)$

OR

Q.2 Simplify the following expression using k-map and realize it using basic gates: **(10)**

a) $F(A,B,C,D) = \sum m(0,1,2,3,5,7,8,9,10,12,13)$

b) $F(A,B,C,D) = \pi M(2,8,9,10,11,12,14)$

Q.3 Draw a logic diagram, block diagram and write a truth table for: **(10)**
a) Half Adder b) Half Subtractor

OR

Q.3 Describe the function of parity bit generators and checkers for even and odd with the help of logic diagram. **(10)**

Q.4 Design and explain 4-bit SISO shift register in detail. **(10)**

OR

Q.4 Describe working of T- flip flop and SR-flip flop with the help of truth table. **(10)**

Q.5 Design a logic diagram to detect the sequence 1010. **(10)**

OR

Q.5 Draw state diagram of S-R, J-K, T and D flip flop. List the rules for state assignment. **(10)**

Q.6 Design and implement Full Adder using Programmable logic Array (PLA). **(10)**

OR

Q.6 Give the classification of memories. **(10)**

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