B-Tech-Sem-III, (2014 course), E&TC
winter-2018

B. Tech. Sem -III (E & TC Engg.) (2014 COURSE) (CBCS) :
WINTER - 2018

SUBJECT: DIGITAL CIRCUITS & APPLICATIONS

Day: Friday
Date: 30/11/2018

Time: 10.00 AM TO 01.00 PM
Max Marks. 60

W-2018-2324

N.B.:
1) All questions are **COMPULSORY.**
2) Figures to the right indicate **FULL** marks
3) Draw the labeled diagrams **WHEREVER** necessary

Q.1 **a)** What is BCD code? Explain the rules for BCD addition with one example **(04)**

b) Minimize the logic function using K map and draw logic diagram **(06)**
$f(A,B,C,D)=\sum m(0,1,2,3,5,7,8,9,11,14)$

OR

a) Convert following decimal numbers into it's equivalent binary numbers **(05)**
I.$(25.75)_{10}$ II.$(115)_{10}$

b) What are Demorgan's theorems? Write them in equation form, prepare their truth tables to prove their correctness **(05)**

Q.2 **a)** Draw 4-bit parallel adder diagram using full adder. **(05)**

b) What is Priority encoder? **(05)**

OR

a) What is comparator? Explain 2 bit magnitude comparator **(05)**

b) What is code converter? Explain any type of code converter **(05)**

Q.3 **a)** What are the characteristics of digital ICs and families? Explain **(05)**

b) Draw And explain the operation of CMOS NOR gate **(05)**

OR

a) Design and explain standard TTL with open collector output configuration **(05)**

b) Draw And explain the operation of CMOS NAND gate **(05)**

Q.4 **a)** What is the difference between latch and flip flop **(03)**

b) Reduce the number of states in the following state tables and draw state diagram for it **(07)**

Present state	Next state		Output	
	X=0	X=1	X=0	X=1
a	f	b	0	0
b	d	c	0	0
c	f	e	0	0
d	g	a	1	0
e	d	c	0	0
f	f	b	1	1
g	g	h	0	1
h	g	a	1	0

P.T.O.

OR

a) Design T flip flop using J-K flip flop **(05)**

b) What is state machine? Explain Mealy and Moore state machines with examples **(05)**

Q.5 **a)** What are types of shift registers? Explain anyone in detail **(05)**

b) Design 4 bit Asynchronous up counter **(05)**

OR

a) What is the difference between Synchronous and Asynchronous counter? **(05)**

b) Design 4 bit Ring counter. **(05)**

Q.6 **a)** A combinational circuit is defined by function **(05)**
$F_1 = \sum m (1,5,7, 9,11,12)$
$F_2 = \sum m (5,6,7,10,11,13,15)$
Implement the circuit with PLA

b) Draw and explain structure of SRAM **(05)**

OR

a) Implement full adder using PROM **(05)**

b) Draw and explain structure of DRAM **(05)**

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B. Tech. sem-III, (2014 course), E&TC
winter-2018

B. Tech. Sem -III (E & TC Engg.) (2014 COURSE) (CBCS) :
WINTER - 2018
SUBJECT : NETWORK THEORY

Day : Monday
Date : 03/12/2018

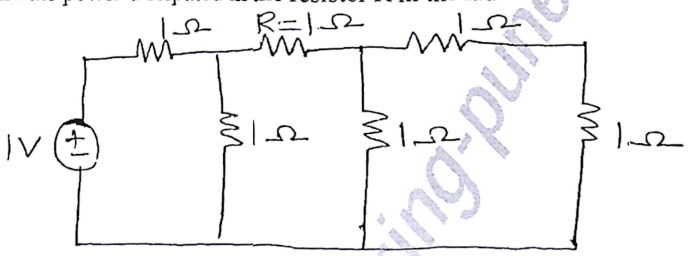
Time : 10.00 AM TO 01.00 PM
Max. Marks : 60

W-2018-2325

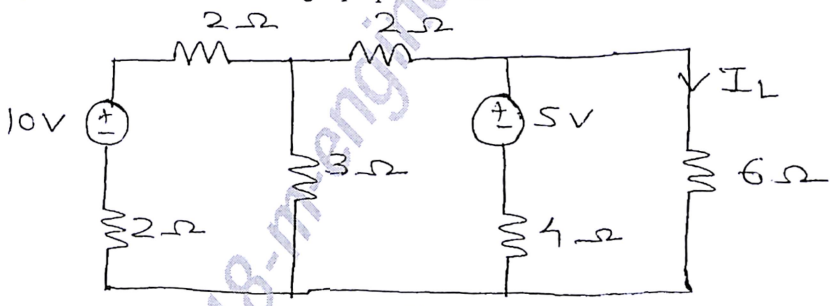
N. B. :

1) All questions are **COMPULSORY**.
2) Figures to the right indicate **FULL** marks.
3) Draw neat and labeled diagram **WHEREVER** necessary.
4) Use of non-programmable calculator is **ALLOWED**.
5) Assume suitable data, if necessary.

Q. 1 a) Find the power dissipated in the resistor R in the ladder network shown: **(05)**

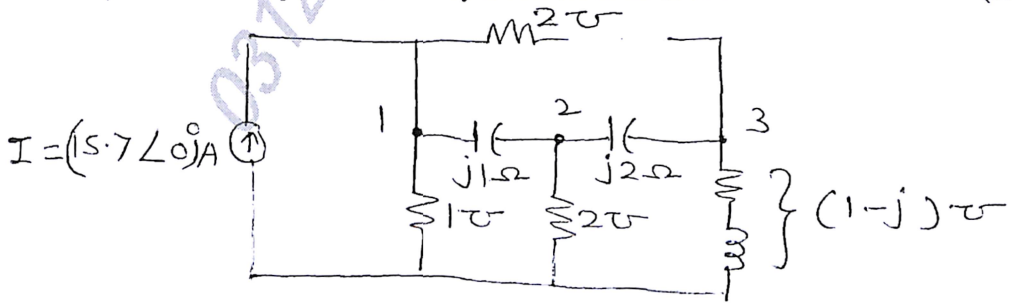


b) Find the load current using superposition theorem. **(05)**

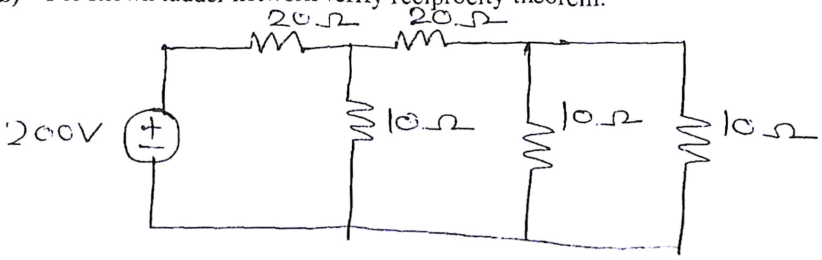


OR

a) Calculate the power delivered by the source in the shown circuit: **(05)**



b) For shown ladder network verify reciprocity theorem: **(05)**



P. T. O.

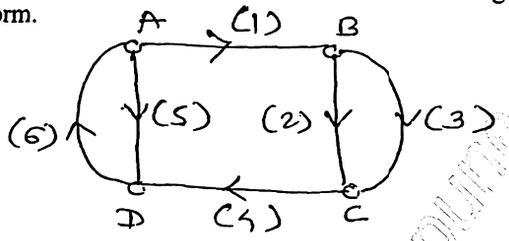
Q. 2 **a)** Complete incidence matrix is given find total No. of trees for the concern matrix graph: **(06)**

$$Aa = \begin{bmatrix} -1 & 0 & 1 & 0 \\ 1 & -1 & 0 & -1 \\ 0 & 1 & 0 & 0 \\ 0 & 0 & -1 & 1 \end{bmatrix}$$

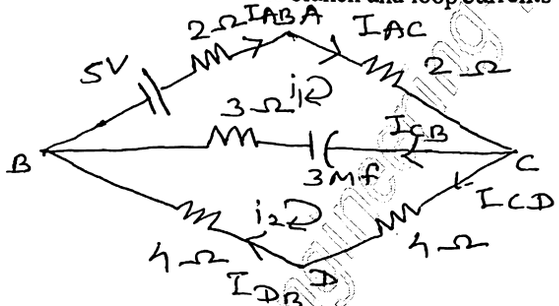
b) What is the condition of Isomarphic graphs? **(04)**

OR

a) What is tieset? Find total No. of tiesets for the following graph and write it in matrix form. **(05)**



b) For the shown network relate branch and loop currents **(05)**



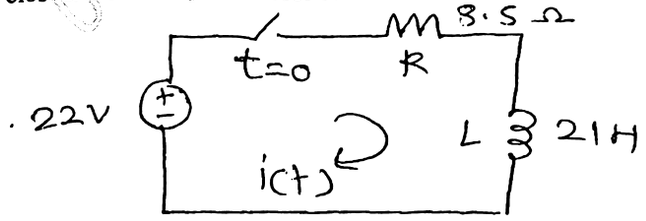
Q. 3 **a)** Find transient response of driven RL circuit. **(05)**

b) For series RC network switch will be closed at $t = 0$ with unchanged capacitor. **(05)**

Find: $i, \frac{di}{dt}, \frac{d^2i}{dt^2}$ *at* $t = 0^+$. *Given*: $R = 2\ k\ \Omega, V = 25v$ *and* $C = 2\mu f$.

OR

a) For the shown network, switch is kept open for long time. At $t = 0$, switch k is closed. Obtain expression for current in the circuit for t > 0. **(05)**



b) Find transient response of undriven RC circuit. **(05)**

Q. 4 **a)** Derive resonating frequency f_r for series RLC circuit. **(04)**

b) A series circuit having capacitor of negligible resistance and coil of 120 μH with 18 Ω resistance at 1 MHz. The circuit is driven by a generator at 1V, 1 MHz frequency with Rg = 0 Ω. What will be the voltage across capacitor? What currents will flow at resonance? **(06)**

OR

a) What is the difference between series and parallel resonant circuit? (05)

b) A parallel circuit has a fixed capacitor and variable inductor having constant quality factor of 4 , find value of inductance and capacitance for circuit impendence of 1 k Ω at resonating frequency 2.4 MHz. (05)

Q. 5 a) Design a constant k-LPF $(T \& \pi)$ with $Fc = 10\,KHz$ and to work with characteristic resistance of 600 Ω. (05)

b) Derive ZOT for m derived filter. (05)

OR

a) Design m low pass T section having design impedance of 600 Ω, a cut off frequency of 2 KHz and a frequency of infinite attenuation of 2100Hz. (05)

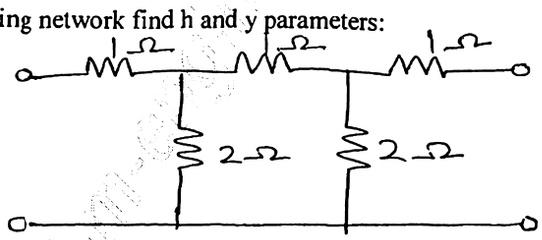
b) What are the design formulae of k BPF? (05)

Q. 6 a) Find symmetry and reciprocity conditions of ABCD parameters. (05)

b) When two networks are connected in series find Z parameter for the combined network? (05)

OR

a) For the following network find h and y parameters: (05)



b) Derive Y parameter in term of h parameter. (05)

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