BACHELOR OF TECHNOLOGY (CBCS - 2023)
B. Tech. Sem-III Computer Science & Engineering : WINTER: 2025
SUBJECT: MACHINE ORGANIZATION & MICROPROCESSORS

Day : Monday
Date : 15/12/2025

W-29204-2025

Time : 10:00 AM-01:00 PM
Max. Marks : 60

NB :
1. Assume suitable data, if necessary.
2. Draw neat labelled diagrams WHEREVER necessary.
3. Figures to the right indicate FULL marks for the question.
4. All questions are COMPULSORY.

Q. 1	Describe the main architectural features of the Intel 80386 microprocessor. Explain the role of its internal units and how they support multitasking and memory management.	(10)
	OR	
Q. 1	What are data movement instructions in the 80386 instruction set? Explain the working of MOV, PUSH, POP, XCHG, and LEA with examples.	(10)
Q. 2	Explain the structure and functionality of the EFLAGS register in the Intel 80386 microprocessor. Describe at least five status and control flags with their significance and effect on program execution.	(10)
	OR	
Q. 2	Compare and contrast segment translation and page translation in the 80386 architecture. Illustrate how both mechanisms work together to convert a logical address into a physical address.	(10)
Q. 3	Describe the function of the Task Register and TSS Descriptor in managing multitasking in the 80386DX microprocessor.	(10)
	OR	
Q. 3	How do segment-level and page-level protections complement each other in the 80386DX architecture? Explain with examples.	(10)
Q. 4	Explain the various I/O addressing techniques supported by the 80386 microprocessor. How does memory-mapped I/O differ from isolated I/O? Illustrate with examples.	(10)
	OR	
Q. 4	Define and explain I/O exceptions. List the different types of exceptions that can occur during I/O operations and how the 80386 handles them.	(10)
Q. 5	What is the Translation Lookaside Buffer (TLB)? Describe how TLB testing can be performed and what debugging mechanisms are useful in identifying TLB-related issues.	(10)
	OR	
Q. 5	Discuss the procedure and significance of switching the 80386 processor from real mode to protected mode. What precautions must be taken?	(10)

Q. 6 Describe the structure of the V86 stack. Illustrate with a diagram how interrupts and exceptions are handled in Virtual 8086 Mode. (10)

OR

Q. 6 Compare the architecture and use cases of microcontrollers with microprocessors. Provide at least three technical and three application-level differences. (10)

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