BACHELOR OF TECHNOLOGY (CBCS) (2021-COURSE)
B. Tech. Sem - II Computer Science & Engineering-AI & ML : WINTER : 2024
SUBJECT: DIGITAL ELECTRONICS

Day : Tuesday
Date : 26/11/2024

W-23932-2024

Time : 10:00 AM-01:00 PM
Max. Marks : 60

N.B.

1) All questions are **COMPULSORY**.
2) Figures to the **RIGHT** indicate **FULL** marks.
3) Use of **non-programmable calculator** is allowed.
4) Assume suitable data **WHEREVER** necessary.
5) Draw neat diagram **WHEREVER** necessary.

Q.1 Define logic gates and discuss the types of logic gates. Explain the functionality of AND, OR, NOT, NAND, NOR gates with truth tables and logic symbol. **(10)**

OR

Q.1 Perform the following conversions:
- **a)** Add 11011 and 10101 **(02)**
- **b)** Subtract 1010 from 11010 **(02)**
- **c)** Multiply $(2C8)_{16}$ by $(B6)_{16}$ **(03)**
- **d)** Divide $(4D0BE)_{16}$ by $(2A)_{16}$ **(03)**

Q.2 Simplify the following expression using Quine Mc Clusky method and realize it using basic gates. **(10)**
$F(A,B,C,D) = \Sigma m(0,3,7,8,9,11,15)$

OR

Q.2 Simplify the following expression using K-map and realize it using basic gates. **(10)**
- **a)** $F(A,B,C,D) = \Sigma m(0,1,2,3,5,7,8,9,10,12,13)$
- **b)** $F(A,B,C,D) = \pi M(2,8,9,10,11,12,14)$

Q.3 Draw a logic diagram, block diagram, and write a k-map simplification from truth table for full Subtractor. **(10)**

OR

Q.3 Explain Digital Comparators in detail. **(10)**

Q.4 Perform the following conversion of flip flops: **(10)**
- **a)** SR-flip flop to JK-flip flop
- **b)** JK flip flop to D-flip flop

OR

Q.4 Design and explain 4-bit PISO shift register in detail. **(10)**

Q.5 Draw state diagram of S-R, J-K, T and D flip flop. List the rules for state assignment. **(10)**

OR

Q.5 Describe basic elements of ASM chart. Give the salient features of ASM chart. **(10)**

Q.6 Design and implement Full Adder using Programmable logic Array (PLA). **(10)**

OR

Q.6 Describe SRAM and DRAM with its advantages and disadvantages. **(10)**

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