BACHELOR OF TECHNOLOGY (C.B.C.S.) (2021-COURSE)
B. Tech. Sem - III Electronics & Communication : WINTER- 2022
SUBJECT : SWICHING THEORY & LOGIC DESIGN

Day : Friday | Time : 10:00 AM-01:00 PM

Date : 09-12-2022 | **W-25324-2022** | Max. Marks : 60

N.B.:

1) All questions are **COMPULSORY**.
2) Figures to the right indicate **FULL** marks.
3) Draw neat and labelled diagram **WHEREVER** necessary.
4) Use of non-programmable **CALCULATOR** is allowed.
5) Assume suitable data if necessary.

Q.1 Prove the following using the Boolean algebraic theorems. **[10]**

a) $A+\overline{A}.B+A.\overline{B}=A+B$

b) $\overline{A}BC+A\overline{B}C+AB\overline{C}+ABC=AB+BC+CA$

OR

Q.1 Realise the following logic equation using $AB+CD=\overline{\overline{AB}.\overline{CD}}$ **[10]**

a) AND and OR gates b) Only NAND gates

Q.2 Minimize the following expression using k-map **[10]**

a) $f(A,B,C,D)=\sum m(1,3,5,8,9,11,15)+d(2,13)$

b) $f(A,B,C,D)=\sum m(1,3,7,11,15)+d(0,2,5)$

OR

Q.2 Prove the following using De-Morgans theorem. **[10]**

a) $AB+CD=\overline{\overline{AB}.\overline{CD}}$ b) $(A+B).(C+D)=\overline{\overline{A+B}+\overline{C+D}}$

Q.3 Design and explain full adder circuit using two half adders and realisation of full adder using NAND-NAND gates. **[10]**

OR

Q.3 Realise the following functions of four variables using: **[10]**

a) 8:1 multiplexers b) 16:1 multiplexer

i) $f_1=\sum m(0,3,5,6,9,10,12,15)$ ii) $f_1=\sum m(0,1,2,3,11,12,14,15)$

Q.4 Design 4 bit binary UP ripple counter. **[10]**

OR

Q.4 Design J-K flip-flop. **[10]**

Q.5 Write a short note on: **[10]**

a) Classification of RAM b) Classification of ROM

OR

Q.5 Compare TTL and CMOS. **[10]**

Q.6 Explain in detail functions and procedures with reference to VLSI. **[10]**

OR

Q.6 Write a short note on: **[10]**

a) Packages of VLSI b) Configuration of VLSI

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