BACHELOR OF TECHNOLOGY (CBCS - 2023)
B. Tech. Sem-I Computer Science & Engineering : WINTER : 2024
SUBJECT: DIGITAL ELECTRONICS

Day : Tuesday
Date : 10/12/2024

W-27609-2024

Time : 10:00 AM-01:00 PM
Max. Marks : 60

N.B.
1) All questions are **COMPULSORY**.
2) Figures to the **RIGHT** indicate **FULL** marks.
3) Assume suitable data **WHEREVER** necessary.
4) Draw neat labeled diagrams **WHEREVER** necessary.

Q.1 Perform the following conversions **(10)**
a) $(375.25)_{10} = (\ )_2$
b) $(253.25)_8 = (\ )_{10}$
c) $(6BA)_{16} = (\ )_2$
d) $(111101101)_2 = (\ )_8$
e) $(10110110101)_2 = (\ )_{16}$

OR

Q.1 Define universal gates and its types in detail. **(10)**

Q.2 Simplify following function using tabulation method(Quine McCluskey) and implement using logic gates **(10)**
$F(A,B,C,D) = \sum m(0, 1, 3, 7, 8, 9, 11, 15)$

OR

Q.2 Simplify following expression using K-map and implement using NAND gates. **(10)**
$F(A,B,C,D) = \sum m(0, 2, 5,6,7, 13) + d(8,10,15)$

Q.3 Describe working of 8:1 Multiplexer with suitable circuit diagram and truth table. **(10)**

OR

Q.3 Design 4-bit binary to gray code converter with suitable diagram. **(10)**

Q.4 Describe various types of flip-flops with truth table and neat diagram. **(10)**

OR

Q.4 Draw the logic diagram for 4-bit asynchronous counter with positive edge triggered flip-flops. Also draw necessary timing diagram. **(10)**

Q.5 Describe notation of ASM chart. Draw ASM chart and state diagram. **(10)**

OR

Q.5 Design a sequence detector to detect sequence 1 1 0 1. **(10)**

Q.6 Implement full adder circuit using PLA(Programmable Logic Array) **(10)**

OR

Q.6 Explain in detail semiconductor memories. **(10)**

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