BACHELOR OF TECHNOLOGY (CBCS - 2023)
B. Tech. Sem-III Computer Science & Engineering AI & ML : WINTER: 2025
SUBJECT: COMPUTER ORGANIZATION & MICROPROCESSORS

Day : Monday
Date : 15/12/2025

W-29208-2025

Time : 10:00 AM-01:00 PM
Max. Marks : 60

N.B.:

1) All questions are **COMPULSORY**.
2) Figures to the right indicate **FULL** marks.
3) Draw neat diagrams **WHEREVER** necessary.
4) Assume suitable data, if necessary.

Q. 1	What do you mean by STORED PROGRAME computers?	**(10)**
	OR	
Q. 1	Given an instruction format MOV, apply different addressing modes to write sample assembly instructions for an 8086 microprocessor.	**(10)**
Q.2	Give a flow chart on BOOTHS Multiplication Algorithm, defining all variables clearly.	**(10)**
	OR	
Q. 2	What do you mean by Instruction Cycle? Give a block diagram indicating all phases of instruction cycle and explain each stage.	**(10)**
Q. 3	One of the Cache Updation policy is "DIRECT mapping". Explain its operation principle and state its advantages and drawback. Use simple and suitable example with graphics.	**(10)**
	OR	
Q. 3	A system is tested for 10 operations, and all are having READING. Cache systems used is resulting 30% MISS case. It is further stated that the average time response of cache is 12 milli seconds, and the main memory is having 75 milli second. Find out average time response of system considering above data.	**(10)**
Q. 4	Giver block diagram of I/O device and explain its working.	**(10)**
	OR	
Q. 4	Give a technical note on SCSI and USB used for Input and output transfer.	**(10)**
Q. 5	What are the features of Hardwired Control Unit?	**(10)**
	OR	
Q. 5	With reference to micro programmed control unit, explain the following "MICRO SEQUENCING", "MICRO ADDRESS"	**(10)**
Q. 6	Give technical note on UMA, NUMA model.	**(10)**
	OR	
Q. 6	Explain how pipelining can be implemented for the following expression. $A[i] = A[i] + B[i]$ for $i = 0$ to $(n-1)$	**(10)**

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