BACHELOR OF TECHNOLOGY (CBCS) (2021-COURSE)
B. Tech. Sem - I CS&E : WINTER : 2023
SUBJECT : DIGITAL ELECTRONICS

Day : Wednesday
Date : 6/12/2023

Time : 10:00 AM-01:00 PM
W-24021-2023
Max. Marks : 60

N.B. :

1) All questions are **COMPULSORY.**
2) Figures to the right indicate **FULL** marks.
3) Assume **Suitable** data, if necessary.
4) Draw neat diagram **WHEREVER** necessary.

Q.1 Perform the following conversions **(10)**

a. $(253.25)_8 = (\quad)_{10}$
b. $(10110.101)_2 = (\quad)_{16}$
c. $(86.64)_{10} = (\quad)_2$
d. $(B92)_{16} = (\quad)_8$
e. $(162.32)_{10} = (\quad)_2$

OR

Q.1 Illustrate NAND and NOR are universal gates with the help of neat logic diagrams. **(10)**

Q.2 Simplify the following function using k-map and implement using logic gates. **(10)**

$f(A,B,C,D) = \sum m\,(1,5,6,7,11,12,13,15)$

OR

Q.2 Simplify the following function using Quine Mc Cluskey method and implement using logic gates. **(10)**

$f(A,B,C,D) = \sum m\,(0,2,3,6,7,8,10,13)$

Q.3 Design 4 bit Gray to Binary code converter. **(10)**

OR

Q.3 Design half and full adders and Subtractor. Write truth tables. **(10)**

Q.4 Describe different types of flip flops with truth tables and circuit diagrams. **(10)**

OR

Q.4 Design and implement mod-7 counter. Draw timing diagram. **(10)**

Q.5 Distinguish between Moore and Mealy model with suitable example. **(10)**

OR

Q.5 Design 3 bit synchronous counter which goes through following states. **(10)**
1 – 3 – 5 – 7 – 1

Q.6 Describe DRAM organization with neat diagram. Why refreshing is required in DRAM? **(10)**

OR

Q.6 A combinational logic is defined by functions **(10)**

$F_1(A,B,C) = \sum m(4,5,7)$ *and* $F_2(A,B,C) = \sum m(3,5,7)$

Implement this circuit using PLA with 3 inputs, 3 product terms and 2 outputs.

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