BACHELOR OF TECHNOLOGY (CBCS) (2021-COURSE)

B. Tech. Sem - II COMPUTER SCIENCE & ENGINEERING AI & ML : SUMMER : 2024

SUBJECT: DIGITAL ELECTRONICS

Day : Thursday
Date : 30/05/2024

S-23932-2024

Time : 10:00 AM-01:00 PM
Max. Marks : 60

N.B.

1) All questions are **COMPULSORY.**
2) Figures to the **RIGHT** indicate **FULL** marks.
3) Use of **non-programmable calculator** is allowed.
4) Assume suitable data **WHEREVER** necessary.
5) Draw neat diagram **WHEREVER** necessary.

Q.1 Why are NAND and NOR gests called Universal gates? Derive AND and OR gates using NAND and NOR gates. **(10)**

OR

Q.1 Perform the following conversions: **(10)**

a) (110111.101010) Binary to Octal
b) (13.15) Decimal to Binary
c) (1034.20) Octal to Decimal
d) (C9D.B4) HEX to Octal
e) (1011001) Gray to Binary

Q.2 Simplify the following expression using K-map and realize it in universal logic.

a) $F(A,B,C,D) = \Sigma m(1,5,6,12,13,14) + d(2,4)$ **(05)**
b) $F(A,B,C,D) = \pi M(0,1,2,3,4,7)$ **(05)**

OR

Q.2 State and prove De Morgan's Theorems. Reduce the expression $\Sigma m(0,2,3,4,5,6)$ using mapping and implement in NAND logic. **(10)**

Q.3 State rules for BCD addition. Design BCD adder using two 4-bit Binary adders. **(10)**

OR

Q.3 Design following 4-bit code converters with the help of truth table and k-map simplification. **(10)**

a) Binary to Gray code converter
b) Gray to Binary code converter

Q.4 Describe working of T-flip flop and SR-flip flop with the help of truth table. **(10)**

OR

Q.4 Differentiate Asynchronous counters and Synchronous counters. Design 2-bit asynchronous counter using flip flops with the help of timing diagram. **(10)**

Q.5 Develop an ASM chart and draw state diagram to detect the sequence 1010. **(10)**

OR

Q.5 Explain the following state machines in detail : **(10)**

a) Moore state machine
b) Mealy state machine

Q.6 Write a short note on : Programmable Logic Devices, Explain any one PLD in detail. **(10)**

OR

Q.6 Give the logic implementation of **(10)**

a) 32 x 4-bit ROM using a decoder of suitable size.
b) 8 x 4-bit ROM using a decoder of suitable size.

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