BACHELOR OF TECHNOLOGY (CBCS) (2021-COURSE)

B. Tech. Sem - II COMPUTER SCIENCE & BUSINESS SYSTEM : WINTER : 2024

SUBJECT: PRINCIPLES OF ELECTRONICS ENGINEERING

Day : Wednesday
Date : 27/11/2024

W-24140-2024

Time : 10:00 AM-01:00 PM
Max. Marks : 60

N.B.

1) All questions are **COMPULSORY**.
2) Figures to the right indicate **FULL** marks.
3) Draw neat and labelled diagram **WHEREVER** necessary.
4) Use of non – programmable **CALCULATOR** is allowed.
5) Assume suitable data if necessary.

Q.1 Draw the atomic structure of P-type extrinsic semiconductor and explain the effect of acceptor impurities on the fermi energy level. **(10)**

OR

Q.1 Explain drift current and diffusion current with the help of diagram in detail. **(10)**

Q.2 Draw and explain V–I characteristics of PN-junction diode. Also compare ideal diode and practical diode. **(10)**

OR

Q.2 Draw and explain working of full wave bridge rectifier with waveforms. Define ripple factor and efficiency for the same circuit. **(10)**

Q.3 Define Transistor and types of transistors. Explain α, β and γ factors of Transistor. Derive the relation between α & β **(10)**

OR

Q.3 Describe stability factors s, s' and s" of transistors. Derive general expression for stability factor. Also state stability factor of fixed bias and voltage divider bias circuits. **(10)**

Q.4 Draw the basic structure and explain the operation of N-channel JFET. Sketch output and transfer characteristics for the same. **(10)**

OR

Q.4 What is the difference between construction of an enhancement type MOSFET and depletion type MOSFET? Also compare JFET and MOSFET. **(10)**

Q.5 Differentiate positive feedback and negative feedback of amplifier. Draw topologies of feedback amplifier. **(10)**

OR

Q.5 Draw and explain application of OP-AMP as constant gain multiplier and voltage follower. **(10)**

Q.6 **a)** State and prove De-Morgan's theorems with the help of truth table and logic diagrams. **(05)**

b) Define universal gates? Implement all basic gates using any one universal gate. **(05)**

OR

Q.6 Draw and explain operation of J–K flip flop using NAND gate. Explain race-around condition. **(10)**

* * *