

**BACHELOR OF TECHNOLOGY (CBCS - 2023)**  
**B. Tech. Sem-IV Computer Science & Engineering : SUMMER : 2025**  
**SUBJECT: COMPUTER ORGANIZATION & ARCHITECTURE**

Day : Thursday  
Date : 29/05/2025

**S-29275-2025**

Time : 10:00 AM-01:00 PM  
Max. Marks : 60

**N.B.**

- 1) All questions are **COMPULSORY**.
- 2) Figures to the **RIGHT** indicate **FULL** marks.
- 3) Assume suitable data **WHEREVER** necessary.
- 4) Draw neat diagrams **WHEREVER** necessary.

**Q. 1** Differentiate between Computer Organization and Architecture. Explain the functional organization of a computer system with a neat block diagram. (10)

**OR**

**Q. 1** Draw and explain in detail the Von-Neumann Architecture of computer. (10)

**Q. 2** Describe Booth's algorithm for signed binary multiplication. Illustrate the algorithm using the example: Multiply  $(-5) \times (-3)$ . (10)

**OR**

**Q. 2** What is Hardwired Control Unit? Draw and explain the working of Sequence Counter Hardwired Control Unit. (10)

**Q. 3** Explain Addressing Mode of an Instruction with the help of examples? Identify the Addressing mode of the following instructions. (10)

1. MOV AL, 25h
2. ADD AX, [BX+SI+02h]
3. CLC
4. SBB CL,[2000h]
5. ADC AL,BL

**OR**

**Q. 3** What is Interrupt? Explain the steps involved in interrupt handling with the help of a diagram. (10)

**Q. 4** Explain the 4-Way Set Associative cache mapping techniques in detail with suitable diagram and example. (10)

**OR**

**Q. 4** Draw and Explain the Memory Hierarchy in Computer. List its features and Application. (10)

**Q. 5** What is Direct Memory Access? How does it help in reducing CPU load? (10)

**OR**

**Q. 5** Draw and explain the architecture of USB. (10)

**Q. 6** With a neat diagram, describe a 5-stage instruction pipeline. Identify and explain each stage. (10)

**OR**

**Q. 6** What is cache coherence in parallel processors? Explain the working of MESI protocol. (10)

\*\*\*\*\*