BACHELOR OF TECHNOLOGY (CBCS - 2023)
B. Tech. Sem-III Computer Science & Business Systems : WINTER : 2024
SUBJECT: COMPUTER ORGANIZATION & ARCHITECTURE

Day : Thursday
Date : 05/12/2024

W-29214-2024

Time : 10:00 AM-01:00 PM
Max. Marks : 60

N.B.

1) All questions are **COMPULSORY.**
2) Figures to the right indicate **FULL** marks.
3) Use of non-programmable calculator is allowed.
4) Assume suitable data if necessary.

Q.1 Explain how Index addressing mode, Immediate addressing mode and Relative addressing mode work? **(10)**

OR

Q.1 Explain the use of the following registers of 8086 CPU: **(10)**
i) General purpose registers **ii)** Segment register
iii) Pointer and index register **iv)** Flag register

Q.2 Draw and explain hardware implementation of Booth's algorithm. **(10)**

OR

Q.2 Design a flowchart for the restoring division algorithm. Implement this algorithm to perform the division of 11 by 3, demonstrating the steps involved in it. **(10)**

Q.3 Demonstrate how multiple bus organization would be applied to optimize the data flow in a processor design for high-performance tasks. **(10)**

OR

Q.3 Explain Single bus organization of the data path inside a processor. Write a control sequence for the given instruction for single bus organization ADD(R3), R1 assuming R1 as destination. **(10)**

Q.4 Explain briefly about associate-mapped and set-associate mapped cache. **(10)**

OR

Q.4 Categorize the different types of memory interleaving techniques used in computer system. **(10)**

Q.5 Illustrate various I/O modes of transfer. **(10)**

OR

Q.5 Write a short note on peripheral devices. With a neat sketch explain the working principle of DMA. **(10)**

Q.6 Explain performance evaluation factors of pipeline processor. **(10)**

OR

Q.6 Explain shared memory parallel processor. **(10)**

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