BACHELOR OF TECHNOLOGY (CBCS) (2021-COURSE)
B. Tech. Sem - I Computer Science & Engineering : WINTER : 2024
SUBJECT: DIGITAL ELECTRONICS

Day : Friday
Date : 06/12/2024

W-24021-2024

Time : 10:00 AM-01:00 PM
Max. Marks : 60

N.B.

1) All questions are **COMPULSORY.**
2) Figures to the **RIGHT** indicate **FULL** marks.
3) Assume suitable data **WHEREVER** necessary.
4) Draw neat labeled diagrams **WHEREVER** necessary.

Q.1 Perform the following conversions **(10)**

a) $(10101101.0111)_2 = (\ )_8$
b) $(615.25)_8 = (\ )_{16}$
c) $(BC66.AF)_{16} = (\ )_8$
d) $(12.125)_{10} = (\ )_2$
e) $(A3E)_{16} = (\ )_{10}$

OR

Q.1 Describe different types of Digital codes and state their application. **(10)**

Q.2 State different Boolean Laws. **(10)**
Simplify following expression using Boolean Laws and implement using logic gates.

i) $Y = (AB + \overline{BC}).C$
ii) $Y = ABC + \overline{A} + A\overline{B}C$

OR

Q.2 Simplify following expressions using tabulation method (Quine McCluskey) and implement using logic gates. **(10)**
$F(A,B,C,D) = \sum m(0, 2, 3, 6, 7, 8, 10, 13)$

Q.3 Design 4 bit Gray to Binary code converter. **(10)**

OR

Q.3 Describe working of 8:1 Multiplexer with suitable circuit diagram and truth table. **(10)**

Q.4 Design 3 bit synchronous up counter and draw neat timing diagram. **(10)**

OR

Q.4 Describe different types of flip-flops with truth tables and circuit diagrams. **(10)**

Q.5 Describe notation of ASM chart. Draw ASM chart and state diagram. **(10)**

OR

Q.5 Design a sequence detector to detect sequence 1 1 0 1. **(10)**

Q.6 Describe architecture of PLA with neat block diagram and explain with suitable example. **(10)**

OR

Q.6 Explain in detail semiconductor memories. **(10)**

*****