BACHELOR OF TECHNOLOGY (CBCS) (2020 COURSE)
B.Tech.Sem - V INFORMATION TECHNOLOGY : WINTER : 2024
SUBJECT: COMPUTER ARCHITECTURE & ORGANIZATION

Day : Friday
Date : 06/12/2024

W-24732-2024

Time : 02:30 PM-05:30 PM
Max. Marks : 60

N.B.

1) All questions are **COMPULSORY**.
2) Figures to the **RIGHT** indicate **FULL** marks.
3) Assume suitable data **WHEREVER** necessary.
4) Draw neat diagrams **WHEREVER** necessary.

Q.1 Explain the following terms in detail and differentiate between them: **(10)**
a) GPU b) TPU c) CPU

OR

Q.1 What is performance metrics? What are the different parameters to measure the performance of the processor? Explain in detail. **(10)**

Q.2 Explain how VHDL code testing is performed with an example. **(10)**

OR

Q.2 Write the VHDL code for 4:1 multiplexer with dataflow and behavioral methods. Mention proper comments. **(10)**

Q.3 Explain the hardwired control unit design using delay element method with neat diagram. **(10)**

OR

Q.3 Give the micro-operations for the execution of JNZ REPEAT instruction. Mention proper comments. **(10)**

Q.4 Explain the set associative cache memory mapping technique with neat diagram. What are the advantages and disadvantages of this method? **(10)**

OR

Q.4 What is cache coherence? Explain the different methods to achieve it. **(10)**

Q.5 What are the different important blocks/elements in the architecture of a supercomputer? Explain with neat diagram. **(10)**

OR

Q.5 Describe the distributed memory-architecture in detail with neat diagram. **(10)**

Q.6 How the performance of a pipeline is evaluated? Explain with examples. **(10)**

OR

Q.6 What is dynamic scheduling? What is out-of-order execution? Why they are important in improving the performance of a processor? Explain with example. **(10)**

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