BACHELOR OF TECHNOLOGY (CBCS) (2021-COURSE)
B. Tech. Sem - II Computer Science & Business Systems : SUMMER : 2025
SUBJECT: PRINCIPLES OF ELECTRONICS ENGINEERING

Day : Tuesday
Date : 03/06/2025
S-24140-2025
Time : 10:00 AM-01:00 PM
Max. Marks : 60

N.B.

1) All questions are **COMPULSORY.**
2) Figures to the right indicate **FULL** marks.
3) Draw neat and labelled diagram **WHEREVER** necessary.
4) Use of non – programmable **CALCULATOR** is allowed.
5) Assume suitable data if necessary.

Q.1 What is mean by Fermi energy level? Draw and explain fermi levels for Intrinsic semiconductor and Extrinsic (P & N type) semiconductor. **(10)**

OR

Q.1 Compare Conductor, Semiconductor and Insulator. Also draw energy band diagrams of the same. **(10)**

Q.2 Draw and explain the formation of depletion region when P-N junction diode is forward biased and reverse biased. What is mean by barrier potential? **(10)**

OR

Q.2 Draw and explain working of Half wave rectifier. Define ripple factor and efficiency for the same circuit. **(10)**

Q.3 What is mean by operating point (Q-point)? Draw the transistor characteristics when Q-point lies near to saturation region, cut-off region and in the active region. **(10)**

OR

Q.3 Draw and explain input and output characteristics of Common Base configuration for NPN transistor. Describe α for CB configuration. **(10)**

Q.4 Explain the construction and operation of P–channel JFET. Draw output and Transfer characteristics for the same. **(10)**

OR

Q.4 Draw and explain construction and working of N–channel enhancement type MOSFET. Also draw drain and transfer characteristics graph. **(10)**

Q.5 What is mean by feedback in Amplifiers? Draw and explain block diagram of Amplifier with feedback. List the advantages of negative feedback. **(10)**

OR

Q.5 Draw and explain OP-AMP as Adder and substractor in detail. **(10)**

Q.6 **a)** Explain the difference between combinational circuits and sequential circuits with example. **(05)**

b) Design Half adder and half substractor using logic gates. **(05)**

OR

Q.6 Draw and explain operation of 4–bit ring counter using J–K flip – flops. **(10)**

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