BACHELOR OF TECHNOLOGY (CBCS) (2021-COURSE)
B. Tech. Sem - II Computer Science & Engineering AI & ML : WINTER: 2025
SUBJECT: DIGITAL ELECTRONICS

Day : Friday
Date : 28/11/2025

W-23932-2025

Time : 10:00 AM-01:00 PM
Max. Marks : 60

N.B.

1) All questions are **COMPULSORY**.
2) Figure to the right indicate **FULL** marks.
3) Use of non – programmable **CALCULATOR** is allowed.
4) Draw neat and labelled diagram **WHEREVER** necessary.

Q.1 Perform the following conversions **(10)**

a) (110111.100010) Binary to Octal
b) (126.15) Decimal to Binary
c) (1234.10) Octal to Decimal
d) (A9C.BD) HEX to Octal
e) (111001) Gray to Binary

OR

Q.1 Why are NAND and NOR gates called universal gates? Derive AND and OR gates using NAND and NOR gates. **(10)**

Q.2 Simplify the following expression using K – map and realize it using basic gates. **(10)**

a) $F(A,B,C,D) = \sum m(0,1,2,3,5,7,8,9,10,12,13)$
b) $F(A,B,C,D) = \pi M(2,8,9,10,11,12,14)$

OR

Q.2 Simplify the following expression using Quine Mc Clusky method and realize it using basic gates. **(10)**
$F(A,B,C,D) = \sum m(0,1,3,7,8,9,11,15)$

Q.3 Draw a logic diagram, block diagram and write a truth table for : **(10)**
a) Half Adder
b) Half Subtractor

OR

Q.3 Describe the function of parity bit generators and checkers for even and odd with the help of logic diagram. **(10)**

Q.4 Differentiate Asynchronous counters and Synchronous counters. Design 2 – bit asynchronous counter using flip flops with the help of timing diagram. **(10)**

OR

Q.4 Design and explain 4 – bit SISO shift register in detail. **(10)**

Q.5 Draw state diagram of S – R, J – K, T and D flip flops. List the rules for state assignment. **(10)**

OR

Q.5 Develop an ASM chart and draw state diagram to detect the sequence 1010. **(10)**

Q.6 Design and Implement Full Adder using Programmable Logic Array (PLA). **(10)**

OR

Q.6 Write a short note on : Programmable logic devices. Explain any one PLD in detail. **(10)**

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