BACHELOR OF TECHNOLOGY (CBCS) (2021-COURSE)
Computer Science & Engineering-AI&ML
B. Tech. Sem - II :SUMMER : 2023
SUBJECT : DIGITAL ELECTRONICS

Day : Tuesday | Time : 10:00 AM-01:00 PM

Date : 30-05-2023 | **S-23932-2023** | Max. Marks : 60

N.B.

1) All questions are **COMPULSORY**.
2) Figure to the right indicate **FULL** marks.
3) Use of non – programmable **CALCULATOR** is allowed.
4) Draw neat and labelled diagram **WHEREVER** necessary.

Q.1 Perform the following conversions **(10)**

a) (110101.101010) Binary to Octal
b) (105.15) Decimal to Binary
c) (4057.06) Octal to Decimal
d) (B9F.AE) HEX to Octal
e) (100011) Gray to Binary

OR

Q.1 Perform the following operations **(10)**

a) Add 1001 and 10101
b) Subtract 1110 from 11110
c) Multiply 1001 by 1110
d) Divide 1011 by 11
e) Subtract 1010 from 1101

Q.2 Simplify the following expression using Quine Mc Clusky method and realize it using basic gates. **(10)**
$F(A,B,C,D) = \sum m(0,1,2,7,8,9,10,11,14,15)$

OR

Q.2 Expand the following terms into Standard form **(10)**

a) $A(\overline{A}+B)(\overline{A}+B+\overline{C})$ to Maxterms

b) $A+B\overline{C}+AB\overline{D}+ABCD$ to minterms

Q.3 Draw a logic diagram, block diagram and write a truth table for : **(10)**
a) Half Adder
b) Half Subtractor

OR

Q.3 Compare Demultiplexer with Decoder. Describe working of 3:8 decoder with neat block diagram and truth table. **(10)**

Q.4 Describe working of D – flip flop and JK – flip flop with the help of truth table. **(10)**

OR

Q.4 Design a synchronous Mod – 6 counter using J – K flip flops. **(10)**

Q.5 Draw state diagram of S – R, J – K, T and D flip flops. List the rules for state assignment. **(10)**

OR

Q.5 Explain Multiplexer Controller Method for 2 – bit Up – counter. **(10)**

Q.6 Describe EEPROM and ROM with its advantages and disadvantages. **(10)**

OR

Q.6 Design and Implement 3 – bit Binary to Gray code converter using PLA. **(10)**

* * *