

BACHELOR OF TECHNOLOGY (CBCS) (2021-COURSE)

Computer Science & Engineering

B. Tech. Sem - I :SUMMER : 2023

SUBJECT : DIGITAL ELECTRONICS

Day : Friday

Time : 10:00 AM-01:00 PM

Date : 12-05-2023

S-24021-2023

Max. Marks : 60

N.B. :

- 1) All questions are **COMPULSORY**.
- 2) Figures to the right indicate **FULL** marks.
- 3) Assume **Suitable** data, if necessary.
- 4) Draw neat diagram **WHEREVER** necessary.

- Q.1 Perform the following conversions (10)
- a. $(635)_8 = ()_{10}$
 - b. $(A3E)_{16} = ()_{10}$
 - c. $(6BA)_{16} = ()_2$
 - d. $(375.25)_{10} = ()_2$
 - e. $(101011.101)_2 = ()_8$
- OR
- Q.1 Describe different types of Digital codes and state their applications. (10)
- Q.2 Simplify the following expressions using k-map and implement using logic gates. (10)
- a. $f(A, B, C, D) = \sum m (0, 2, 5, 6, 7, 8, 10, 13, 15)$
 - b. $f(A, B, C, D) = \prod M (0, 1, 2, 4, 5)$
- OR
- Q.2 State the different Boolean laws. Simplify the following expressions using Boolean laws and implement using logic gates. (10)
- a. $y = ABC + \bar{A} + \bar{A}BC$
 - b. $y = (AB + BC)C$
- Q.3 Describe the working of Digital Comparator and Parity Generator. (10)
- OR
- Q.3 Differentiate between Multiplexer and DeMultiplexer. Implement the following function using 8:1 Multiplexer (10)
- $$f(A, B, C, D) = \sum m (0, 3, 4, 7, 8, 9, 13, 14)$$
- Q.4 Describe different modes of Shift Register and explain its applications. (10)
- OR
- Q.4 Design 3 bit Synchronous up counter and draw neat timing diagram. (10)
- Q.5 Describe notations of ASM chart. Draw ASM chart and state diagram for 3 bit up down counter. (10)
- OR
- Q.5 Describe ASM techniques of designing sequential circuit. How does it differ from conventional flow chart? (10)
- Q.6 Describe memory organization of DRAM. Compare SRAM with DRAM. (10)
- OR
- Q.6 Describe architecture of PLA with neat block diagram. Design BCD to Gray code converter using PLA. (10)

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