

**BACHELOR OF TECHNOLOGY (CBCS) (2021-COURSE)**  
**B. Tech. Sem - III COMPUTER SCIENCE & ENGINEERING : SUMMER : 2024**  
**SUBJECT: MACHINE ORGANIZATION & MICROPROCESSOR**

Day : Tuesday  
Date : 14/05/2024

S-25312-2024

Time : 02:30 PM-05:30 PM  
Max. Marks : 60

N.B.:

- 1) All questions are **COMPULSORY**.
- 2) Figures to the right indicate **FULL** marks.
- 3) Use of **CALCULATOR** is allowed.
- 4) Draw neat and labeled diagrams **WHEREVER** necessary.

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- Q.1 Draw and explain flag register of 8086. (10)  
OR  
Differentiate between different types of instructions in the 8086-instruction set with suitable example. (10)
- Q.2 Discuss the principals of floating-point arithmetic and IEEE 754 standard for floating-point representation. Explain the format of IEEE 754 floating-point numbers and the operations defined for floating-point arithmetic. (10)  
OR  
Convert following floating-point binary number into decimal number=011010000000011 assume 9 bits for exponents. (10)
- Q.3 Describe classification of micro instruction execution. Draw structure of vertical micro instructions. (10)  
OR  
Describe the purpose of Control Unit with neat sketch diagram and explain the organization of Hardwired Control Unit. (10)
- Q.4 Define Cache memory and analyze the three-mapping function of cache memory. (10)  
OR  
Explain the concept of memory hierarchy and its significance in modern computer systems. Discuss the characteristics of different levels of memory in the hierarchy, highlighting the trade-off speed, size and cost. (10)
- Q.5 A) Describe micro-instruction sequencing. (05)  
B) Differentiate between Horizontal and Vertical micro-instructions (05)  
OR  
Describe various SCIS Bus Signals and its phases. (10)
- Q.6 Compare and contrast closely and loosely coupled multiprocessor systems, highlighting their respective advantages and limitations in terms of scalability, fault tolerance and communication overhead. (10)  
OR  
Explain the concept of instruction pipelining and its role in improving performance. Discuss the stages involved in instruction pipeline and how hazards are mitigated. Provide examples to illustrate the benefits of instruction pipelining in enhancing CPU throughput. (10)

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