

BACHELOR OF TECHNOLOGY (CBCS) (2021-COURSE)
B. Tech. Sem - II Computer Science & Engineering AI & ML : SUMMER : 2025
SUBJECT: DIGITAL ELECTRONICS

Day : Friday
Date : 30/05/2025

S-23932-2025

Time : 10:00 AM-01:00 PM
Max. Marks : 60

N.B.

- 1) All questions are **COMPULSORY**.
- 2) Figures to the **RIGHT** indicate **FULL** marks.
- 3) Use of **non-programmable calculator** is allowed.
- 4) Assume suitable data **WHEREVER** necessary.
- 5) Draw neat diagram **WHEREVER** necessary.

- Q.1** Perform the following conversions: (10)
- a) (100101.111010) Binary to Octal
 - b) (20.25) Decimal to Binary
 - c) (3156.04) Octal to Decimal
 - d) (CDF.4E) HEX to Octal
 - e) (1110011) Gray to Binary

OR

- Q.1** Perform the following binary operation using 2's complement method.
- a) Add (-75) to (+26) (02)
 - b) Subtract (14) from (46) (02)
 - c) Add (-45.75) to (+87.5) (03)
 - d) Add (-31.5) to (-93.125) (03)

- Q.2** Simplify the following expression using Quine Mc Clusky method and realize it using basic gates. (10)
 $F(A, B, C, D) = \sum m(0, 1, 2, 7, 8, 9, 10, 11, 14, 15)$

OR

- Q.2** a) Expand $A(\bar{A}+B)(\bar{A}+B+C)$ to Maxterms. (05)
b) Expand $A+B\bar{C}+AB\bar{D}+ABCD$ to minterms. (05)
- Q.3** Draw a logic diagram, block diagram, and write a truth table for : (10)
- a) Half Adder
 - b) Half Subtractor

OR

- Q.3** Describe the function of parity bit generators and checkers for even and odd with the help of logic diagram. (10)

- Q.4** Describe working of D-flip flop and JK-flip flop with the help of truth table. (10)

OR

- Q.4** Differentiate Asynchronous counters and Synchronous counters. Design 2-bit asynchronous counter using flip flops with the help of timing diagram. (10)

- Q.5** Design a logic diagram for the serial binary adders. (10)

OR

- Q.5** Design a logic diagram to detect the sequence 1010. (10)

- Q.6** Design and implement 3-bit Binary to Gray code converter using PLA. (10)

OR

- Q.6** Write a short note on: Programmable Logic Devices. Explain any one PLD in detail. (10)

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