BACHELOR OF TECHNOLOGY (CBCS - 2023)

B. Tech. Sem-II COMPUTER SCIENCE & ENGINEERING-A&M : SUMMER : 2024

SUBJECT: DIGITAL ELECTRONICS

Day : Tuesday
Date : 28/05/2024

S-27702-2024

Time : 10:00 AM-01:00 PM
Max. Marks : 60

N.B.

1) All questions are **COMPULSORY**.
2) Figures to the **RIGHT** indicate **FULL** marks.
3) Assume suitable data **WHEREVER** necessary.
4) Draw neat labeled diagrams **WHEREVER** necessary.

Q.1 Perform the following binary operation using 2's complement method.

a) Add (-75) to (+26) **(02)**
b) Subtract (14) from (46) **(02)**
c) Add (-45.75) to (+87.5) **(03)**
d) Add (-31.5) to (-93.125) **(03)**

OR

Q.1 Explain the concept of various digital codes such as BCD code, Excess-3 code, Gray code, and ASCII code. Provide examples to illustrate each code. **(10)**

Q.2 State and prove De-morgan's Theorems. **(10)**
Reduce the expression $\sum m(0,2,3,4,5,6)$ using mapping and implement in NAND logic.

OR

Q.2 Simplify the following expression using K-map and realize it using basic gates.

a) $F(A,B,C,D) = \sum m\ (0,1,2,3,5,7,8,9,10,12,13)$ **(05)**
b) $F(A,B,C,D) = \pi M\ (2,8,9,10,11,12,14)$ **(05)**

Q.3 Compare Demultiplexer with Decoder. Describe working of 3:8 decoder with neat block diagram and truth table. **(10)**

OR

Q.3 Draw a logic diagram, block diagram, and write a k-map simplification from truth table for full subtractor. **(10)**

Q.4 Perform the following conversion of flip flops: **(10)**
a) SR-flip flop to JK-flip flop.
b) JK-flip flop to D-flip flop.

OR

Q.4 Design and explain 4-bit SISO shift register in detail. **(10)**

Q.5 Design a logic diagram for the serial binary adder. **(10)**

OR

Q.5 Describe basic elements of ASM chart. Give the salient features of ASM chart. **(10)**

Q.6 Design and Implement 3-bit Binary to Gray code converter using PLA. **(10)**

OR

Q.6 Classify and explain the semiconductor Memories. Write the characteristics of semiconductor memories. **(10)**

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