BACHELOR OF TECHNOLOGY (CBCS - 2023)
B. Tech. Sem-II Computer Science & Engineering AI & ML : WINTER: 2025
SUBJECT: DIGITAL ELECTRONICS

Day : Wednesday
Date : 26/11/2025

W-27702-2025

Time : 10:00 AM-01:00 PM
Max. Marks : 60

N.B.

1) All questions are **COMPULSORY**.
2) Figures to the **RIGHT** indicate **FULL** marks.
3) Assume suitable data **WHEREVER** necessary.
4) Draw neat diagrams **WHEREVER** necessary.

Q.1 Perform the following conversions:

a) (110101.110010) Binary to Octal (02)

b) (bDF.3E) HEX to Octal (02)

c) (305.15) Decimal to Binary (02)

d) (1010011) Gray to Binary (02)

e) (4136.14) Octal to Decimal (02)

OR

Q.1 Realize the following function using universal logic gates.

a) X-OR (05)
b) X-NOR (05)

Q.2 Simplify the following expression using Quine Mc Clusky method and realize it using basic gates. (10)

$$F(A,B,C,D)=\sum m(0,1,2,7,8,9,10,11,14,15)$$

OR

Q.2 State and prove De Morgan's Theorems. (10)
Reduce the expression $\sum m(0,2,3,4,5,6)$ using mapping and implement in NAND logic.

Q.3 Compare Demultiplexer with Decoder. Describe working of 3:8 decoder with neat block diagram and truth table. (10)

OR

Q.3 Draw a logic diagram, block diagram, and write a k-map simplification from truth table for full Adder. (10)

Q.4 Design a synchronous Mod-6 counter using J-K flip flops. (10)

OR

Q.4 Perform the following conversions of flip flops:

a) SR-flip flop to JK- flip flop (05)

b) JK flip flop to D-flip flop (05)

(PTO)

Q.5 Design a logic diagram to detect the sequence 1010. (10)

OR

Q.5 Draw state diagram of S-R, J-K, T and D flip flop. List the rules for state assignment. (10)

Q.6 Describe SRAM and DRAM with its advantages and disadvantages. (10)

OR

Q.6 Write a short note on: Programmable Logic Devices. Explain any one PLD in detail. (10)

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