B. Tech- sem-V, (2007 course), Computer winter-2018

B.Tech Sem – V (2007 Course) (Computer Engg.) : WINTER - 2018

SUBJECT : COMPUTER ORGANIZATION

Day : Thursday
Date : 29/11/2018

W-2018-2800

Time : 02.30 PM TO 05.30 PM
Max. Marks : 80

N. B. :

1) **Q. No. 1** and **Q. No. 5** are **COMPULSORY**. Out of remaining attempt **ANY TWO** questions from Section – **I** and Section – **II**.
2) Figures to the right indicate **FULL** marks.
3) Answers to both the sections should be written in the **SEPARATE** answer books.
4) Draw neat and labeled diagram **WHEREVER** necessary.
5) Assume suitable data, if necessary.

SECTION - I

Q. 1 a) Describe how the problem of cache coherence is resolved in multiprocessor system. **(06)**

b) Represent the following numbers in single and double precision formats **(04)**
i) (671.25) ii) (0.155)

c) Explain the basic components of CPU. **(04)**

Q. 2 a) Define bus interconnection. List and explain the types of bus interconnection. **(06)**

b) Explain register addressing modes with an example. **(07)**

Q. 3 a) Explain restoring method of division with an example. **(07)**

b) Explain Booth's algorithm for multiplication in detail. **(06)**

Q. 4 a) Explain the EFLAG register of 80386 in detail. **(07)**

b) Explain addressing modes of 80386 in detail **(06)**

SECTION – II

Q. 5 a) Explain micro-instruction sequencing and micro-instruction execution. **(04)**

b) List and explain the characteristics of memory systems. **(05)**

c) Compare closely coupled and loosely coupled multiprocessor configuration. **(05)**

Q. 6 a) Write control sequence for following instruction in single bus organization **(07)**
SUB [R1], R2
where R1 is source address register and R2 is destination register.

b) Describe micro program control. Explain the advantages and disadvantages of hardwired control over micro program control. **(06)**

Q. 7 a) Explain DMA controller with neat diagram. **(07)**

b) Describe Pentium cache organization. **(06)**

Q. 8 a) Define superscalar processor. Explain the features of superscalar processor. **(07)**

b) Describe the design considerations of multiprocessor systems. **(06)**

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