BACHELOR OF TECHNOLOGY (CBCS - 2023)
B. Tech. Sem-I Computer Science & Engineering : WINTER: 2025
SUBJECT: DIGITAL ELECTRONICS

Day : Tuesday
Date : 16/12/2025

W-27609-2025

Time : 10:00 AM-01:00 PM
Max. Marks : 60

N.B.:

1) All questions are **COMPULSORY**.
2) Figures to the right indicate **FULL** marks.
3) Draw neat labelled diagrams **WHEREVER** necessary.
4) Use of non-programmable **CALCULATOR** is allowed.

Q.1 Convert the following: (10)

i) $(10.25)_{10} = (?)_2$
ii) $(152.25)_8 = (?)_{10}$
iii) $(101101.\ 10101)_2 = (?)_{16}$
iv) $(2CD.2F)_{16} = (?)_2$

OR

Q.1 Illustrate NAND and NOR are universal gates with the help of neat logic diagrams. (10)

Q.2 Simplify the following expression using k-map and implement using logic gates. (10)
$f(A,B,C,D) = \sum m(1,5,6,7,11,12,13,15)$

OR

Q.2 Simplify the following using Quine Mc Cluskey method and implement using logic gates. (10)
$f(A,B,C,D) = \sum m(0,1,3,7,8,9,11,15)$

Q.3 Design 4 bit Binary to Gray code converter. (10)

OR

Q.3 Differentiate between multiplexer and demultiplexer. Implement the given function using 8:1 multiplexer. (10)
$f(A,B,C,D) = \sum m(0,3,4,7,8,9,13,14)$

Q.4 Explain in detail J-K flip-flop with neat diagram, excitation table, characteristics table and equation. (10)

OR

Q.4 Illustrate ripple counter in detail. (10)

Q.5 Describe notations of ASM chart. Draw ASM chart and state diagram for 3 bit. (10)

OR

Q.5 Distinguish between Moore and Mealy state machine with suitable diagram. (10)

Q.6 Classify semiconductor memories in detail. (10)

OR

Q.6 Explain architecture of PLA with neat diagram. (10)

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